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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
FR000011

In Re Application Of: **Gesnot**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/773,147	**01/31/2001**	**Thompson, James A.**	**23550**	**2624**	**5941**

Invention: **IMPROVED METHOD OF REDUCING BLOCKING ARTIFACTS**

COMMISSIONER FOR PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:
March 13, 2006

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Dated: **May 10, 2006**

John A. Merecki
Reg. No. 35,812

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Gesnot
Serial No.:	09/773,147
Filed:	January 31, 2001
For:	Improved Method of Reducing Blocking Artifacts
Attorney Dkt. No.:	FR000011
Art Unit:	2624
Examiner:	Thompson, James A.

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BRIEF OF APPELLANTS

This is an appeal from the Final Office Action dated December 12, 2005, rejecting claims 1-4. This Brief is accompanied by the requisite fee set forth in 37 C.F.R. 1.17 (c).

REAL PARTY IN INTEREST

Koninklijke Philips Electronics N.V. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

As filed, this case included claims 1-4. Claims 1-4 remain pending, stand rejected, and form the basis of this appeal.

STATUS OF AMENDMENTS

An After-Final Amendment has not been filed in response to the Final Office Action mailed December 12, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention discloses a simple and efficient method of processing a digital signal for reducing blocking artifacts, without an *a priori* knowledge of the encoding parameters of the input signal. The input signal (IS) is comprised of blocks (see, e.g., blocks p, p+1, FIG. 3a), wherein the blocks comprise n-bit binary input samples, with n being an integer. A low pass filtering step is applied to the input signal, which results in a filtered signal comprising filtered samples (page 3, line 32 - page 4, line 2; FIG. 3c). A determination step is performed for determining a correction area around block boundaries (page 4, lines 3 – 16; FIG. 3d). The determination step includes computing mask values (MV) associated with the input samples using the filtered samples, where the correction area corresponds to an area where the mask values are different from zero. A correction step is performed (page 4, lines 22-25; FIG. 3e) in which a random binary number is added to the filtered samples, which results in an output signal (OS).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claim 1 is unpatentable under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461).
2. Whether claim 2 is unpatentable under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461) and Jung (US 5,732,159).
3. Whether claim 3-4 are unpatentable under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461) and Nakaya (US 6,295,376).

ARGUMENT

(1) Rejection of claim 1 under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461).

Appellant respectfully submit that the rejection of claim 1 under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461) is defective.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

In this case, the rejection is defective because, *inter alia,* Moronaga and Yamada, taken alone or in combination, fail to teach or suggest each and every feature of claim 1 as required by 35 U.S.C. 103(a).

In the Final Office Action (page 4, lines 11-13), the Examiner alleges that the claimed step of "computing mask values" is disclosed in column 11, lines 21-23 of Moronaga. This is incorrect. On the contrary, the cited section of Moronaga is completely silent with regard to the **computing of mask values** associated with the input samples. Further, the cited section of Moronaga is completely silent with regard to the **computing of mask values** associated with the input samples **using filtered samples obtained by filtering an input signal** as in claim 1.

The Examiner further alleges (Final Office Action, page 4, lines 8+) that the claimed step of determining a "correction area corresponding to an area where the mask values are different from zero" is disclosed in column 4, lines 9-16 of Moronaga. This is also incorrect. First, this cited section (column 4, lines 9-16) of Moronaga refers to a first embodiment of Moronaga's image signal regenerating device, while the previously cited section (column 11, lines 21-23) of Moronaga refers to another, entirely different embodiment of Moronaga's image signal regenerating device. Thus, the Examiner has indiscriminately combined, without any supporting rationale, features from different embodiments of Moronaga' image signal regenerating device. Regardless, the section in Moronaga cited by the Examiner (column 4, lines 9-16) is completely silent with regard to a correction area corresponding to an "area where the mask values are different from zero" as set forth in claim 1 of the present patent application.

The Examiner admits (Final Office Action, page 5, lines 10-12) that Moronaga "does not disclose expressly that the mask values associated with the input samples are computed using the filtered samples." To overcome this deficiency of Moronaga,

the Examiner relies on the teachings of Yamada. In particular, the Examiner states (Final Office Action, page 5, lines 13-16) that "Yamada discloses using a low pass filter (figure 1(11) of Yamada) to obtain filtered values (figure 1 (Sus) and column 11, lines 53-59 of Yamada) which are then used to compute mask values (Sorg-Sus) associated with the input samples (Sorg)." Appellant disagrees and submits that since Moronaga does not disclose mask values, there is absolutely no motivation for combining Moronaga and Yamada in the manner suggested by the Examiner.

(2) Rejection of claim 2 under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461) and Jung (US 5,732,159).

Appellant respectfully submits that dependent claim 2 is allowable for reasons similar to those set forth with regard to independent claim 1. Further, contrary to the assertions of the Examiner, Jung does not disclose, *inter alia*, "computing sub-step of mask values equal to the m-n least significant bits of the filtered samples, and said correction step adding the random binary number to the filtered samples divided by the power of 2 when the mask values are different from zero, which results in the output signal." In addition, based on the lengthy and convoluted discussion presented by the Examiner with regard to Jung, it is clear that the Examiner is using impermissible hindsight to "force-fit" and combine the teachings of Jung with those of Moronaga and Yamada.

(3) Rejection of claims 3-4 under 35 U.S.C. 103(a) over Moronaga (US 5,229,864) in view of Yamada (US 5,953,461) and Nakaya (US 6,295,376).

Appellant respectfully submits that dependent claims 3-4 are allowable for reasons similar to those set forth with regard to independent claim 1.

In view of the foregoing, it is respectfully submitted that the currently-pending claims are in condition for allowance, and favorable consideration is earnestly solicited.

Respectfully submitted,

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Date: 5/10/06

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CLAIMS APPENDIX

1. A method of processing an input signal, said input signal comprising blocks and said blocks comprising n-bit binary input samples, with n being an integer, said method of processing comprising at least :

- a low pass filtering step applied to the input signal, which results in a filtered signal comprising filtered samples,
- a determination step for determining a correction area around block boundaries, said determination step including computing mask values associated with the input samples using the filtered samples, said correction area corresponding to an area where the mask values are different from zero, and
- a correction step for adding a random binary number comprising at least one bit to the filtered samples belonging to the correction area, which results in an output signal.

2. A method of processing according to claim 1, also comprising a step of multiplying the input samples by a power of 2, which results in a modified signal comprising modified samples of m-bit binary numbers, said filtering step being applied to the modified signal around block boundaries, said determination step comprising a computing sub-step of mask values equal to the m-n least significant bits of the filtered samples, and said correction step adding the random binary number to the filtered samples divided by the power of 2 when the mask values are different from zero, which results in the output signal.

3. A computer program product for a television receiver that comprises a set of instructions, which, when loaded into the television receiver causes the television receiver to carry out the method as claimed in claim 1.

4. A computer program product for a set-top-box that comprises a set of instructions, which, when loaded into the set-top-box causes the set-top-box to carry out the method as claimed in claim 1.

EVIDENCE APPENDIX

No evidence has been submitted.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.